CLAIMS

1. (Amended) A TFT array substrate, comprising:

a thin film transistor section in which a gate electrode is formed on a substrate, and a semiconductor layer is formed on the gate electrode via a gate insulation layer,

the processed semiconductor layer having a shape formed by dropping a droplet.

2. The TFT array substrate as set forth in claim 1, wherein:

the gate electrode in the thin film transistor section is a branch electrode which is branched out of a main line of the gate electrode, and the branch electrode has an open end protruded from an area for the semiconductor layer.

3. The TFT array substrate as set forth in claim 2, wherein:

the branch electrode is arranged so that a portion protruded from the area for the semiconductor layer is smaller in width than a portion confined within the area for the semiconductor layer.

4. The TFT array substrate as set forth in claim 2,

wherein:

AMENDED SHEETS

the thin film transistor section further includes a source electrode and a drain electrode on the semiconductor layer, and a channel section is formed between the source and drain electrodes, and the portion of the branch electrode protruded from the area for the semiconductor layer is formed in contact with one of the source and drain electrodes.

5. The TFT array substrate as set forth in claim 2, wherein:

the thin film transistor section further includes a source electrode and a drain electrode on the semiconductor layer, and a channel section is formed between the source and drain electrodes, and the portion of the branch electrode protruded from the area for the semiconductor layer is formed according to the following formula (1),

$$L3 > r + \Delta 1 + 2\Delta 2 \quad \ldots (1)$$

where r denotes a distance from a center of the channel section to an outermost end of the channel section, $\Delta 1$ denotes a first error taking account of variation of dropping amount of the droplet for forming the semiconductor layer and variation of spread of the droplet after dropping, $\Delta 2$ denotes a second error taking account of dropping off a target position, and L3 denotes a distance from the center of the channel section to the open end of the branch electrode.

6. The TFT array substrate as set forth in claim 2, wherein:

the thin film transistor section further includes a source electrode and a drain electrode on the semiconductor layer, and a channel section is formed between the source and drain electrodes, and the portion of the branch electrode protruded from the area for the semiconductor layer is formed according to the following formula (2),

$$L2 > \Delta 1 + 2\Delta 2 \quad \ldots (2)$$

where $\Delta 1$ denotes a first error taking account of variation of dropping amount of the droplet for forming the semiconductor layer and variation of spread of the droplet after dropping, $\Delta 2$ denotes a second error taking account of dropping off a target position, and L2 denotes a distance from (1) an end of each of the source and drain electrodes, closer to the open end of the branch electrode, to (2) the open end of the branch electrode.

7. The TFT array substrate as set forth in claim 1, wherein:

the thin film transistor section further includes a source electrode and a drain electrode on the semiconductor layer, and a channel section is formed between the source and drain electrodes, and the source and drain electrodes each have an end that is positioned closer to the channel section, and

confined over an entire width within the area for the semiconductor layer.

8. The TFT array substrate as set forth in claim 1, wherein:

the thin film transistor section further includes a light-blocking film on either of an upper layer or an lower layer of the semiconductor layer, the light-blocking film having a shape formed by dropping a droplet, and being formed on a portion corresponding to the position of the semiconductor layer.

9. The TFT array substrate as set forth in claim 1, wherein:

the thin film transistor section further includes a source electrode and a drain electrode on the semiconductor layer, and a channel section is formed between the source and drain electrodes, and the semiconductor layer is formed according to the following formula (3),

$$R > r + \Delta 1 + \Delta 2 \quad \ldots (3)$$

where r denotes a distance from a center of the channel section to an outermost end of the channel section, $\Delta 1$ denotes a first error taking account of variation of dropping amount of the droplet for forming the semiconductor layer and variation of spread of the droplet after dropping, $\Delta 2$

denotes a second error taking account of dropping off a target position, and R denotes a radius of the semiconductor layer, which extends from the center of the channel section.

10. A liquid crystal display device including the TFT array substrate as set forth in claim 1.

11. A manufacturing method of a TFT array substrate, comprising the steps of:

(a) forming a gate electrode on a substrate;

(b) forming a gate insulation layer on the gate electrode;

(c) depositing a semiconductor film on the gate insulation layer;

(d) forming a resist layer having a shape of a droplet by dropping a droplet of a resist material on the semiconductor film; and

(e) removing the resist layer, after processing the semiconductor film corresponding to the shape of the resist layer so as to create a semiconductor layer of a thin film transistor section.

12. The manufacturing method of a TFT array substrate as set forth in claim 11, wherein:

in the step (a), the gate electrode is formed so that the gate electrode includes a main line and a branch electrode

branched out of the main line, the branch electrode having an open end protruded from an area for the semiconductor layer.

13. The manufacturing method of a TFT array substrate as set forth in claim 12, wherein:

the branch electrode is specified by length according to dropping accuracy of the droplet so that the open end is protruded from the area for the semiconductor layer.

14. The manufacturing method of a TFT array substrate as set forth in claim 12, wherein:

the branch electrode is formed so that a portion protruded from the area for the semiconductor layer is smaller in width than a portion confined within the area for the semiconductor layer.

15. The manufacturing method of a TFT array substrate as set forth in claim 12, wherein:

the portion of the branch electrode protruded from the area for the semiconductor layer is formed in contact with one of source and drain electrodes of the thin film transistor section.

16. The manufacturing method of a TFT array substrate as set forth in claim 12, wherein:

in the step (a), the branch electrode is formed so that a portion protruded from the area for the semiconductor layer is formed according to the following formula (1),

$$L3 > r + \Delta 1 + 2\Delta 2 \quad \ldots (1)$$

where r denotes a distance from a center of the channel section to an outermost end of the channel section, Δ1 denotes a first error taking account of variation of dropping amount of the droplet for forming the semiconductor layer and variation of spread of the droplet after dropping, Δ2 denotes a second error taking account of dropping off a target position, and L3 denotes a distance from the center of the channel section to the open end of the branch electrode.

17. The manufacturing method of a TFT array substrate as set forth in claim 13, wherein:

in the step (a), the branch electrode is formed so that a portion protruded from the area for the semiconductor layer is formed according to the following formula (2),

$$L2 > \Delta 1 + 2\Delta 2 \quad \ldots (2)$$

where Δ1 denotes a first error taking account of variation of dropping amount of the droplet for forming the semiconductor layer and variation of spread of the droplet after dropping, Δ2 denotes a second error taking account of dropping off a target position, and L2 denotes a distance from (1) an end of each of the source and drain electrodes, closer

to the open end of the branch electrode, to (2) the open end of the branch electrode.

18. The manufacturing method of a TFT array substrate as set forth in claim 11, wherein:

in the step (d), the resist layer is formed according to the following formula (3),

$$R > r + \Delta 1 + \Delta 2 \quad \ldots (3)$$

where r denotes a distance from a center of the channel section to an outermost end of the channel section, $\Delta 1$ denotes a first error taking account of variation of dropping amount of the droplet for forming the semiconductor layer and variation of spread of the droplet after dropping, $\Delta 2$ denotes a second error taking account of dropping off a target position, and R denotes a radius of the semiconductor layer, which extends from the center of the channel section.

19. A manufacturing method of a TFT array substrate, comprising the steps of:

(a) forming a gate electrode with a branch electrode on a substrate;

(b) forming a gate insulation layer on the gate electrode; and

(c) forming a semiconductor layer having a shape of a droplet as a semiconductor layer of a thin film transistor

section, by dropping a droplet of a semiconductor material on the gate insulation layer on the branch electrode.

20. The manufacturing method of a TFT array substrate as set forth in claim 19, wherein:

in the step (a), the gate electrode is formed so that the gate electrode includes a main line and a branch electrode branched out of the main line, the branch electrode having an open end protruded from an area for the semiconductor layer.

21. The manufacturing method of a TFT array substrate as set forth in claim 19, wherein:

the step (c) includes the sub-steps of:

(i) depositing a semiconductor film on the gate insulation layer;

(ii) forming a resist layer having a shape of a droplet by dropping a droplet of a resist material on the semiconductor film; and

(iii) removing the resist layer, after processing the semiconductor film corresponding to the shape of the resist layer so as to create a semiconductor layer of a thin film transistor section, and

in the step (ii), the resist layer is formed according to the following formula (3),

$$R > r + \Delta 1 + \Delta 2 \quad \ldots (3)$$

where r denotes a distance from a center of the channel section to an outermost end of the channel section, Δ1 denotes a first error taking account of variation of dropping amount of the droplet for forming the semiconductor layer and variation of spread of the droplet after dropping, Δ2 denotes a second error taking account of dropping off a target position, and R denotes a radius of the semiconductor layer, which extends from the center of the channel section.

22. A manufacturing method of a TFT array substrate, comprising the steps of:

(a) forming a gate electrode on a substrate;

(b) forming a gate insulation layer on the gate electrode;

(c) forming a semiconductor layer of a thin film transistor section on the gate insulation layer;

(d) forming a first area to which a source electrode is formed, and a second area to which at least a pixel electrode is formed, by dropping a droplet of an electrode material on the substrate after subjected to the step (c); and

(e) forming a source electrode, a drain electrode, and a pixel electrode in the first and the second areas by dropping droplets of an electrode material on the substrate after subjected to the step (d).

23. The manufacturing method of a TFT array substrate

as set forth in claim 22, wherein:

the first and the second areas are provided by forming a convex guide which prevents flow of the droplet.

24. The manufacturing method of a TFT array substrate as set forth in claim 22, wherein:

the first and the second areas are provided by forming a lyophilic area and a lyophobic area respectively having a lyophilic characteristic and a lyophobic characteristic with respect to the droplets.

25. A manufacturing method of a liquid crystal display device including the manufacturing method of a TFT substrate as set forth in claim 11.

26. A TFT array substrate, comprising:

a thin film transistor section in which a gate electrode is formed on a substrate, and a semiconductor layer and a conductor layer are formed on the gate electrode via a gate insulation layer,

wherein:

the conductor layer is formed in contact with the semiconductor layer and one of source and drain electrodes of the thin film transistor section, and has a portion formed by dropping a droplet, the conductor layer and the

semiconductor layer having substantially the same shape in the portion formed by dropping a droplet.

27. The manufacturing method of a TFT array substrate as set forth in claim 26, wherein:

the conductor layer is constituted of Mo, W, Ag, Cr, Ta, Ti, a metal material mainly containing one of Mo, W, Ag, Cr, Ta, Ti, or an indium tin oxide.

28. The manufacturing method of a TFT array substrate as set forth in claim 27, wherein:

the source and drain electrodes are made of an Al or a metal material mainly containing Al.

29. A liquid crystal display device including the TFT array substrate as set forth in claim 26.

30. A manufacturing method of a TFT array substrate, comprising the steps of:

(a) forming a gate electrode on a substrate;

(b) forming a gate insulation layer on the gate electrode;

(c) depositing a semiconductor film on the gate insulation layer;

(d) forming a conductor forming layer having a shape of a droplet by dropping a droplet of a conductive material on

the semiconductor film; and

(e) forming a semiconductor layer of a thin film transistor section by processing the semiconductor film corresponding to the shape of the conductor forming layer.

31. The manufacturing method of a TFT array substrate as set forth in claim 30, further comprising the step of:

processing the conductor forming layer so as to form a conductor layer,

wherein:

the conductor layer is constituted of Mo, W, Ag, Cr, Ta, Ti, a metal material mainly containing one of Mo, W, Ag, Cr, Ta, Ti, or an indium tin oxide.

32. The manufacturing method of a TFT array substrate as set forth in claim 31, wherein:

the source and drain electrodes are made of an Al or a metal material mainly containing Al.

33. A manufacturing method of a liquid crystal display device including the manufacturing method of a TFT substrate as set forth in claim 30.

34. An electronic device including the TFT array substrate as set forth in claim 1.

35. An electronic device including the TFT array substrate as set forth in claim 26.